

B1.4-R3: COMPUTER ORGANIZATION

NOTE:

1. There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.
2. **PART ONE** is to be answered in the **TEAR-OFF ANSWER SHEET** only, attached to the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.
3. Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

TOTAL TIME: 3 HOURS

TOTAL MARKS: 100
(PART ONE – 40; PART TWO – 60)

PART ONE **(Answer all the questions)**

1. **Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the “tear-off” answer sheet attached to the question paper, following instructions therein.** (1 x 10)
 - 1.1 Normally digital computers are based on
 - A) AND and OR gates
 - B) NAND and NOR gates
 - C) NOT gate
 - D) None of the above
 - 1.2 Logic families of IC having dense packing density, simpler processing techniques and more economic operations are
 - A) TTL
 - B) ECL
 - C) CMOS
 - D) None of the above
 - 1.3 The smallest number which can be represented as signed number (using 2's compliment) in 2 bytes is
 - A) -2^{15}
 - B) $-2^{15} + 1$
 - C) 0
 - D) None of the above
 - 1.4 Which one does not change the information content during movement of binary information in registers?
 - A) Register transfer micro-operations
 - B) Arithmetic operations
 - C) Logic operations
 - D) None of the above

- 1.5 The most efficient method for translating arithmetic expressions into machine language instructions is using
- A) prefix notations
 - B) postfix notations
 - C) infix notations
 - D) none of the above
- 1.6 One of the multiplication algorithms is
- A) Restoring method
 - B) Comparison method
 - C) Booth's algorithm
 - D) None of the above
- 1.7 Synchronization mechanism in I/O operation is needed because
- A) Nature of operations of peripherals are different from operations of CPU and memory
 - B) The data transfer rate of peripherals is usually slower than the transfer rate of the CPU
 - C) Operation modes of peripherals are different from each other
 - D) None of the above
- 1.8 Locality of reference refers to
- A) scope of local variables in functions
 - B) the area in the memory where the address of instruction is stored
 - C) the fact that reference to memory at any given interval of time, during the program execution tends to confine with in few localized area in the memory
 - D) none of the above
- 1.9 Instructions performing actions in assembly language are called
- A) Imperative statements
 - B) Declarative statements
 - C) Directive statements
 - D) None of the above
- 1.10 Address and content of memory word are stored in
- A) Set associative mapping
 - B) Associative mapping
 - C) Direct mapping
 - D) None of the above

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the “tear-off” sheet attached to the question paper, following instructions therein. (1 x 10)

- 2.1 Gates may have more than two inputs.
- 2.2 Decoders are constructed with OR gates.
- 2.3 In representation of signed number using 1’s compliment, zero does not have unique representation.
- 2.4 The address of the next instruction to be executed is available in IR.
- 2.5 On interrupt, CPU may abandon the execution of current instruction in middle.
- 2.6 In hardware algorithm (restore), partial remainder is restored by adding the divisor to the negative difference.
- 2.7 Usually parallel transmission is used for short distance.
- 2.8 Disks may have simultaneous transfer of bits from several tracks at the same time.
- 2.9 Extra segment in assembly language is used only in exceptional condition.
- 2.10 In set associative memory, each word of cache can store two or more words of memory under the same index address.

3. Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the “tear-off” answer sheet attached to the question paper, following instructions therein. (1 x 10)

X		Y	
3.1	Combinational circuit performing arithmetic addition of three bits	A.	Sequential adder
3.2	Read – control lines not needed	B.	normalized
3.3	Non-zero most significant digit of mantissa of floating – point number	C.	Full adder
3.4	Basic component of arithmetic circuit	D.	RAM
3.5	Memory address not required	E.	Half adder
3.6	Multiplication operands are in 2’s compliment representation	F.	subroutine
3.7	Similar to data transfer between CPU interface units	G.	Strobe transfer
3.8	A memory unit accessed by content	H.	Indirect addressing
3.9	Body of it expanded and assembled every time it is encountered in the program	I.	Parallel adder
3.10	Several programs reside in memory	J.	Signed bit
		K.	ROM
		L.	Booth’s algorithm
		M.	Associative memory
		N.	Memory stack
		O.	Macro
		P.	Virtual memory
		Q.	Multiprogramming
		R.	Handshake
		S.	Comparison method

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the “tear-off” answer sheet attached to the question paper, following instructions therein. (1 x 10)

A.	instruction register	B.	port	C.	SP
D.	IP	E.	virtual	F.	complement
G.	initial	H.	ROM	I.	JK flip-flop
J.	data selector	K.	does not indicate	L.	indicate
M.	immediate	N.	indirect	O.	condition code
P.	program status word	Q.	multiplexer	R.	SR

- 4.1 Indeterminate condition is there in _____.
- 4.2 _____ is another name for multiplexer.
- 4.3 In addition of two signed numbers, sign bit is treated as part of number and the end carry _____ an overflow.
- 4.4 In _____ instruction, actual operand is present instead of address.
- 4.5 The collection of all status bit conditions in CPU is called _____.
- 4.6 The subtraction operation can be achieved through _____ and add.
- 4.7 Data register in I/O interface unit is called _____.
- 4.8 Bootstrap loader is stored in _____ portion of memory.
- 4.9 _____ memory gives illusion of large memory.
- 4.10 Offset value of address of instruction is kept in _____.

PART TWO
(Answer any **FOUR** questions)

- 5.**
- a) What is binary counter? Why T and JK flip-flops are employed in counter circuit? Give the circuit diagram of 4 bit synchronous binary counter.
 - b) What is multiplexer? What are functions of multiplexer inputs? Draw logic diagram of 4 to 1 line multiplexer giving function table also.

(7+8)

- 6.**
- a) What is the purpose of shift micro operation? Explain different types of shifts.
 - b) How is a program executed in computer? List steps associated with each instruction cycle. Explain Fetch and Decode phase. Draw the block diagram of a register transfer for fetch phase.

(7+8)

- 7.**
- a) Explain Booth's multiplication algorithm using a flow chart. Draw the configuration for the hardware implementation of Booth's algorithm.
 - b) What is U A R T? What is baud rate? Consider a serial transmission whose transfer rate is 9 characters per second. The system uses 2 stop bits and has eight signaling states. Calculate its baud rate.

(7+8)

- 8.**
- a) What is the principle of locality of reference? How is this idea utilized in cache memory? What is the basic operation of cache? What is hit ratio? Suppose a computer with cache access time of 100 ns, a main memory access time of 1000 ns, what will be the average access time if hit ratio is .n.
 - b) Write an assembly language program segment to find the largest number among 50 numbers, which are stored consecutively at **NUM**, which is defined as word.

(7+8)

- 9.**
- a) Explain Hardware algorithm for division using flow chart. What is divide overflow problem and how is it handled?
 - b) Given 128 x 8 RAM & 512 x 8 ROM chips
 - i) How many chips are needed to provide a memory capacity of 512 bytes of RAM & 512 bytes of ROM?
 - ii) How many lines of address bus must be used to access the above mentioned memory address map?
 - iii) How will you differentiate between a RAM & ROM address?

(6+9)